DESIGN OF HIGH-PERFORMANCE ULTRASONIC PHASED ARRAY EMISSION AND RECEPTION CONTROLLING SYSTEM

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Abstract - Ultrasonic phased array inspection technology is widely used in the nondestructive testing field, while its implementation is uneasy because of the precise phase controlling demanded both in emitting and in receiving process as well as the real-time mass data processing during echo reception. This paper designs and realizes an FPGA-based high-performance ultrasonic phased array emission and reception controlling and processing system. The system’s emitting controller is capable of emitting square-shaped triggering waves of 64 independent channels at most and 1ns time-delay resolution each channel by utilizing precise timing control functions in FPGA. Furthermore, the emitting controller achieves to emit arbitrary-shaped triggering waves of finite length in 1ns time-delay resolution and sinusoidal waves in finer time-delay resolution by combining high-performance DACs with direct digital synthesis technology supported in FPGA. The system’s reception processor manages to achieve up to 64-channel high-speed high-precision real-time echo sampling and subsequent parallel digital signal processing by using high-performance ADCs and FPGAs. Testing and research indicate that the system has a good performance in the aspects of precise timing control and real-time mass data processing during the continuous emitting and receiving procedure, meeting the versatile applications’ requirements of ultrasonic phased array inspection technology.

1. Introduction

The first industrial ultrasonic phased array inspection instruments, introduced in the 1980s, were used for in-service power generation inspections. Later, phased array technology became prevalent in industrial fields as modern industrial testing required, along with the continuous development of electronic technology.1,2

The phase delay resolution of ultrasonic phased array controlling and processing system has a great influence on the instruments’ inspection resolution. In early designs, analog delay line was employed to achieve the phase delay during the procedure of both emitting and receiving, which made the system extremely large and also the inaccuracy and coarseness of phase control. Nowadays, as the transition into the digital world, one of the solutions of ultrasonic phased array inspection instruments that high-performance field programmable gate array (FPGA) can be used to achieve digital time delay at nanosecond level by the switching of logic state. Furthermore, finer
time delay resolution is feasible if we combine direct digital synthesis (DDS) technology embedded in FPGA with digital-to-analog converter (DAC).

How to handle the real-time mass data generated as digitalization technology applied in instruments is another difficulty in design, besides the phase delay. Thanks to the increase of working frequency of FPGA and the powerfulness of digital signal processing (DSP) units and high-speed serial interfaces embedded in FPGA, it’s now available to process and transmit the real-time mass data during inspection.

Thus, the high-performance ultrasonic phased array controlling and processing system lays a solid foundation to high-performance ultrasonic phased array inspection instruments. In this paper, we designed and realized an FPGA-based high-performance ultrasonic phased array emission and reception controlling and processing system.

2. System Design

The system is designed to realize the function of 64-channel ultrasonic phased array low-voltage triggering wave emission as well as echo sampling and processing, excluding the amplification of triggering wave to excitation wave imposed on the transducers and the amplification of echo from microvolt or millivolt level to volt level.

The system composes of several kinds of boards, shown in Fig. 1. The first kind is a standard 6U CPCI specification system board, where the self-designed ultrasonic phased array inspection software, which won’t be presented in this paper, is installed. Clock board generates systematic clock and synchronization signals for Board #1 to Board #8, named as data board, and receives the beamforming data from them to upload to system board. The data boards are identical on hardware configurations; each controls the emission and reception procedures of 8 channels, adding up to 64 in total. Also, there is a self-designed backplane board for the former boards to plug in. Both CPCI bus and high-speed serial bus is adopted on the backplane board, which the former is used for the registers configuration in FPGAs on data boards by the software on system board and the later is designed for the transmission of beamforming data among clock board and data boards. Besides the interconnections in the rear end on backplane board, there are coaxial cable connections in the front end to deliver systematic clock and synchronization signals from clock board to data boards.

![Figure 1. System architecture and interconnections](image)

Data board is vital to the system performance. There are 2 Xilinx Virtex-5 FPGAs installed on each data board as the controlling and processing cores, shown in Fig. 2. The right one is in charge of emission procedure, achieving the emission of multiple kinds of low-voltage triggering waves through input/output interfaces or combined with DACs’ outputs. And the left one is responsible for reception procedure, controlling the sampling of ADCs and the processing of sampled echo data.

The system is roughly working as follows:

1. When power’s on, clock board supplies clock signals to data boards. Users set the focal law and some other parameters by software to all the FPGAs through CPCI bus.
2. During the inspection, clock board generates synchronization signals to data boards. Simultaneously, data boards control the emission and reception procedure, which should be communicating with the analog circuits and transducers.

3. There are two working modes: real time and non-real time. In real time mode, each data board carries out digital beamforming of 8 channels, and transmit the data to clock board through high-speed serial bus to further beamforming of more channels if needed, then uploads the data to the software through CPCI bus for display and simple analysis. While in non-real time mode, data boards store the entire echo data to the DDR2 SDRAM chips connected to FPGAs temporarily, and the software will access the data for complicate analysis when enough data is stored.

2.1 Emission Controlling

Phase control is realized by time delay in ultrasonic phased array. Specifically, truncation errors lead to the generation of side lobes because of the discrete of time delay. And time delay resolution influences the beam steering and focal control directly. Thus, time delay resolution affects the system’s contrast resolution and spatial resolution significantly. We made a deliberate design to implement the high-precision control that each data board has a dedicated FPGA to manage the time delay emission of triggering waves.

Generally, most of commercial ultrasonic phased array inspection instruments support only negative pulse or square wave of excitation wave to the transducer, which both can be triggered by the identical CMOS level square-shaped triggering wave, i.e., logic signal. While, for the purpose of further research, low-voltage arbitrary-shaped triggering wave is introduced in our system. For example, it will be useful in research of ultrasonic phased array time reverse technology, if the arbitrary-shaped triggering wave can be amplified lossless to the level of exciting the phased array transducer.

2.1.1 Square-shaped Triggering Wave

CMOS level logic signal accords with the standard of FPGA’s input/output interfaces. Xilinx Virtex-5 FPGA’s output interfaces have the OSERDES resources. OSERDES, short for output serializer/deserializer, is a dedicated parallel-to-serial converter. We programmed the logic resources at the clock of 250MHz, setting the data serialization to 4:1. Then, the output interfaces run at the clock of 500MHz, configured in double data rate (DDR) mode, to implement the 1ns time delay resolution. Here the 4-bit data is computed in every cycle of 250MHz clock, according to the focal law and width value prewritten in the random access memory (RAM) resources in FPGA.
2.1.2 Arbitrary-shaped Triggering Wave

Arbitrary-shaped triggering wave is analog, which means DACs needed to convert the FPGA’s digital outputs to analog waves. We choose a 16-bit, 1.0 GSPS 2x-4x interpolating dual-channel DAC and each data board contains 4 DAC chips.

We store the digitalized arbitrary-shaped wave data into the RAM resources in FPGA before inspection. When the synchronization signal for emission from clock board is received, the wave data is accessed and formed by the programmed logic to send to the DAC chips. Specifically, the time delay control is implemented in two steps. First, the fine time delay resolution is 1ns at the range of 0~3ns and it’s achieved by invoking the different starting position of the wave data. Second, the programmed logic runs at the clock of 250MHz, delaying the wave data in the unit of 4ns by using the first-in first-out (FIFO) resources in FPGA. A FIFO of 2048 words depth is used that the dynamic range of coarse time delay is 8192ns.

DAC’s analog output voltage range of each channel is 1V peak to peak and 0V offset when a 50Ohm resistance is matched. The analog output is coupled to an SMA connector by a transformer whose pass band is from 60 kHz to 300MHz.

2.1.3 Sinusoidal Triggering Wave

In the case of arbitrary-shaped triggering wave, the wave length is limited because of the size of RAM resources in FPGA. Now, we consider a particular situation that the triggering wave is sinusoidal.

DDS modules in FPGA are instantiated to generate the sinusoidal wave data for DACs. Phase controlled sinusoidal wave of different frequency can be acquired by configuring the PINC and POFF registers in DDS module.4

The data width of DDS module is 16-bit according to the data width of DAC. Thus, the total number of phase steps amounts to 65536, which means each step corresponds to 0.061 picoseconds of time delay at the clock of 250MHz. Obviously, it’s impossible and needless to utilizing such precise time delay because of the jitter of the clock signal and some other factors. But, it would be possible to achieve time delay resolution at the level of 100 picoseconds.

2.2 Reception Controlling and Processing

2.2.1 Echo Sampling

Before the amplified echoes are transmitted into the FPGAs, they have to be converted from analog to digital by ADCs. We choose a 14-bit, 250MSPS dual-channel ADC but configure the maximum sampling frequency at 200MHz. Each data board contains 4 ADC chips.

The amplified echo is inputted by an SMA connector each channel, and is coupled to be differential signal by a transformer whose pass band is 250 kHz to 750MHz. The ADC’s analog input interface accepts the differential signal at the maximum voltage range of 2V peak to peak. The dedicated FPGA, controlling the reception procedure, manages the configuration of ADCs and receives the converted data from ADCs during inspection.

2.2.2 Echo Data Processing

Generally, the basic operation of ultrasonic phased array echo data processing is digital beam-forming, further including dynamic apodization, dynamic focusing and multi-beamforming, etc. In real time mode, these operations should be executed in FPGA by weighting, delaying and summing of the echo data and also filtering and compacting if needed.5 ,6

Similarly, the time delay in reception procedure is also divided into two parts: coarse time delay and fine time delay. At the clock of 200MHz, by utilizing the build-in FIFO resources, FPGA delays the echo data at some certain cycles decided by the focal law to achieve coarse time delay of 5ns as a unit. While the fine time delay is achieved by linear interpolating the echo data at the inter-
val of 1ns but only the exact one of every five points decided by the focal law is kept to remain the data rate at 200MSPS. A basic beamforming is accomplished when we sum the delayed echo data.

Dynamic apodization can be realized by weighting the delayed echo data before summing, shown in Fig. 3. Dynamic focusing and multi-beamforming require the processing of the echo data for multiple times, calling the different focal laws prewritten in RAM resources in FPGA. Nowadays, high-performance FPGAs abound in logic cells and storage resources, fitting for full parallel processing.

Figure 3. The block diagram of the digital beamformer of 8 channels

2.2.3 Beamforming Data Transmission

The backplane supplies high-speed serial bus interconnections for Beamforming data transmission within system. The Gigabit Transceiver with Low Power (GTP) embedded in FPGA is the high-speed serial interface we adopted. And Aurora 8B/10B whose top data transmission rate reached up to 3.125Gb/s per channel is the protocol we used to transfer data. 7

In real time mode, we execute the beamforming on single data board firstly, and then put the data together from two adjacent data boards through one Aurora 8B/10B channel, followed by transmitting to the clock board through two Aurora 8B/10B channels each on four data boards, shown in Fig. 4.

Figure 4. High-speed serial bus connections in system

The FPGA installed on clock board receives the beamforming data from 8 data boards and carries out further beamforming of more channels if needed and upload the data for display and simple analysis to the software on system board through CPCI bus.

3. System Performance Analysis and Testing

We used Tektronix Digital Phosphor Oscilloscope 7254C to measure the 1ns time delay resolution of arbitrary-shaped triggering wave. Four random channels were chosen to be measured, which shared the identical wave data prewritten in the RAM resources in FPGA. Firstly, four channels emitted the triggering wave at the very same time, shown in Fig. 5(a). Then, the outputs were
configured with 1ns interval, shown in Fig. 5(b). Coaxial cables were used to connect the triggering wave output connectors to the oscilloscope, leading to the instinct bias of approximate ±100ps between channels.

Figure 5. a) Four channels emit the triggering wave simultaneously; b) Four channels emit one by one at interval of 1ns. The time axis scale is 1ns/div.

We both simulated and tested the function of digital beamforming logical module. Full parallel computing is introduced, so the real-time processing in single FPGA on single board has an excellent performance. Figure 6 illustrates a simulation of 8-channel digital beamforming. The top 8 quantized analog waves represent pseudo echo wave data sampled by ADCs, and the bottom one indicates the beamforming data, which is acquired by summing the fine and coarse time delayed echo data.

Figure 6. A simulation of the 8-channel digital beamformer.

4. Conclusion

This paper designed and realized a FPGA-based high-performance ultrasonic phased array emission and reception controlling and processing system. The system adopts the CPCI bus architecture, facilitating communications between system board and self-designed boards, combined with high-speed serial bus for real-time transmission of mass beamforming data. We took full advantage of the abilities of timing control, logical calculation and full parallel computing in FPGA to realize 64 channels of emission triggering wave output at 1ns time delay resolution and 64 channels of amplified echo sampling as well as processing.
The system is suitable for general industrial ultrasonic phased array inspection. It aims at the scientific experiments and research in industrial fields of ultrasonic phased array testing and imaging, and will boost both the basic and the cutting-edge research related. The system also provides an effective solution to similar high-performance commercial product design.

REFERENCES


